UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,539	01/30/2002	Jung-Chcun Lien	ACT-317	3903

28661 7590 10/19/2006

SIERRA PATENT GROUP, LTD.
1657 Hwy 395, Suite 202
Minden, NV 89423

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 10/066,539	Applicant(s) LIEN ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 are pending and have been examined. Claims 1-4 have been amended.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/15/2006 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1-5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

<u>Claims 1-4:</u>

Regarding claim 1 the phrase "such that", which is similar to "such as", renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d). This should be changed to "...applied <u>to the</u> adjacent...".

<u>Claim 5:</u>

This claim is also rejected because it depends on claim 4 and has the same problems of indefiniteness.

<u>Claim 1:</u>

The newly amended claim limitation "wherein said set of test inputs are applied such that adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values" renders the claim indefinite because, as read, the Examiner interprets that the test inputs are applied to the adjacent tracks in the first set of tracks and the adjacent tracks in the second set of tracks <u>at the same time</u>, whereas the cited pages and line numbers of the specification (Page 29, lines 8-18 and Page 30, lines 5-15) implies that this is done <u>at different times</u>. Correction and clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici et al. (US-6108806), hereinafter Abramovici, in view of Andrews et al. (US-6064225), hereinafter Andrews, in further view of Kean (US-6292018), hereinafter Kean, in even further view of Das et al. (A Low Cost Approach for Detecting, Locating, and Avoiding Interconnect Fault in FPGA-Based Reconfigurable Systems), hereinafter Das.

<u>Claim 1:</u>

Abramovici teaches test pattern generators 20 which generate test patterns (defining a set of test inputs) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici also teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response (determining/obtaining an expected output). Abramovici also teaches the third and seventh rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (comparing said expected results with said actual results) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response

analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col. 5, lines 20-22, Col 6, lines 1-5, 17-23, 30, 31). Abramovici teaches that a field programmable gate array (FPGA) is a type of integrated circuit consisting of an array of programmable logic blocks (PLBs) interconnected by programmable routing resources and programmable I/O cells (plurality of interface groups (IGs)) and, in programming these logic blocks, routing resources and I/O cells is selectively completed to make the necessary interconnections (provide signals to said routing circuitry) that establish a configuration thereof to provide desired system operation/function for a particular circuit application. (Col. 1, ll. 21-28). Abramovici does not explicitly teach "each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile" and "a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs". Abramovici does teach, as stated above, the FPGA consists of PLBs and programmable I/O cells (plurality of interface groups (IGs)). Andrews teaches a conventional field programmable gate array (FPGA) 100, consisting of an array of programmable logic cells (PLCs) 102 surrounded by a ring of programmable input/output (I/O) cells (PICs) 104 (plurality of interface groups (IGs)), where the PICs handle the flow of data into and out of the PLC array (provide signals to said routing circuitry). Andrews also teaches each PIC has four pads (e.g., 210) connected to the inputs of a four-to-one mux (e.g., 212) (each of said IGs having a plurality of input

multiplexers configurable to select signals received from outside of said FPGA tile and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers). Andrews further teaches for each PIC, the output of the mux is connected to a global-signal spine (e.g., 214) that carries global signals from the PIC to perpendicular branches (e.g., 216) that correspond to rows in the PLC array and provide programmable connections to the individual PLCs (provide signals to said routing circuitry). (Col. 1, ll. 10-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's programmable I/O cells (IGs) with Andrews' PICs. The artisan would have been motivated to do so because this would enable Abramovici to selectively route signals from outside of the FPGA to the PLCs and other programmable logic blocks.

Abramovici does not explicitly teach providing a global control signal which turns on all interconnect elements simultaneously. However, Abramovici does teach the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU (first set of tracks) and a second BTU (second set of tracks), which have separate test pattern generators 20 driving each one. Abramovici also teaches communicating of test patterns generated by the test pattern generators to the programmable logic blocks under test by global routing (global control signals). Kean teaches in an analogous art a global control signal which turns on all interconnect elements simultaneously of a CALII FPGA which supports arrangement of the control store and the use of the wildcard registers and shift and mask registers which minimizes the number of microprocessor

instructions required to access device resources and status. The specific structure of the control store allows many control bits to be written simultaneously instead of one at a time because of the structured set of data in the RAM. (Col. 43, ll. 52-66, col. 29, ll. 31-40, col. 7, ll. 39-43, col. 25, l. 63 to col. 26, l. 25, col 28, ll. 19-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's FPGA to utilize Kean's CAL II FPGA and to adopt Keans's simultaneous activation of the control bits as to simultaneously turn on the interconnect elements. The artisan would be motivated to do so because it would enable Abramovici to minimize reconfiguration time reducing the cost of device testing where a large number of configurations is required.

Abramovici does not explicitly teach "said set of test inputs are applied such that adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values". However, Abramovici does teach output response generators 24 comparing adjacent BUT outputs. Das teaches in an analogous art "applying a set of test inputs to the adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values" in that "[t]o diagnose bridging faults between two nets (**adjacent tracks**), complementary values (**different logic values**) have to be driven on the nets and each net has to be observed at the output (**obtaining actual results...**)". (See page 267, section 2, col. 1, page 269, section "Bridging fault between two nets", col. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enhance Abramovici's FPGA interconnection testing method with Das's

interconnection testing method to find stuck-at and bridging faults. The artisan would be motivated to do so because it would enable Abramovici to fully test the programmable interconnect exactly as it will be used in system operation. Bridging faults between all pairs of nets are both detected and located greatly increasing the dependability of Abramovici's reconfigurable system (FPGA) with low cost. (See Das, page 270, section 6. Conclusions).

Claim 2 and 3:

Abramovici teaches that the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU (first set of tracks, per claim 2) and a second BTU (second set of tracks, per claim 3), which have separate test pattern generators 20 driving each one. Abramovici also teaches test pattern generators 20 which generate test patterns (plurality of signal sources) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici further teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response. Abramovici also teaches the third and seventh rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (producing expected output values) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch

signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col 4, lines 25-30, 44-55; Col. 5, lines 20-22; Col 6, lines 1-5, 17-23, 30, 31). Abramovici teaches that a field programmable gate array (FPGA) is a type of integrated circuit consisting of an array of programmable logic blocks (PLBs) interconnected by programmable routing resources and <u>programmable I/O cells</u> (plurality of interface groups (IGs)) and, in programming these logic blocks, routing resources and I/O cells is selectively completed to <u>make the necessary interconnections</u> (provide signals to said routing circuitry) that establish a configuration thereof to provide desired system operation/function for a particular circuit application. (Col. 1, ll. 21-28). Abramovici does not explicitly teach "each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile" and "a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs". Abramovici does teach, as stated above, the FPGA consists of PLBs and <u>programmable I/O cells</u> (plurality of interface groups (IGs)). Andrews teaches a conventional field programmable gate array (FPGA) 100, consisting of an array of programmable logic cells (PLCs) 102 surrounded by a ring of programmable input/output (I/O) cells (PICs) 104 (plurality of interface groups (IGs)), where the PICs handle the flow of data into and out of the PLC array (provide signals to said routing circuitry). Andrews also teaches each PIC has four pads (e.g., 210) connected to the inputs of a four-to-one mux (e.g., 212) (each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and a plurality of input/output pads (I/Os) coupled to at least

one of said input multiplexers). Andrews further teaches for each PIC, the output of the mux is connected to a global-signal spine (e.g., 214) that carries global signals from the PIC to perpendicular branches (e.g., 216) that correspond to rows in the PLC array and provide programmable connections to the individual PLCs (provide signals to said routing circuitry). (Col. 1, ll. 10-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's programmable I/O cells (IGs) with Andrews' PICs. The artisan would have been motivated to do so because this would enable Abramovici to selectively route signals from outside of the FPGA to the PLCs and other programmable logic blocks.

Abramovici does not explicitly teach providing a global control signal which turns on all interconnect elements simultaneously. However, Abramovici does teach the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU (first set of tracks) and a second BTU (second set of tracks), which have separate test pattern generators 20 driving each one. Abramovici also teaches communicating of test patterns generated by the test pattern generators to the programmable logic blocks under test by global routing (global control signals). Kean teaches in an analogous art a global control signal which turns on all interconnect elements simultaneously of a CALII FPGA which supports arrangement of the control store and the use of the wildcard registers and shift and mask registers which minimizes the number of microprocessor instructions required to access device resources and status. The specific structure of the control store allows many <u>control bits to be written simultaneously</u> instead of one at

a time because of the structured set of data in the RAM. (Col. 43, ll. 52-66, col. 29, ll. 31-40, col. 7, ll. 39-43, col. 25, l. 63 to col. 26, l. 25, col 28, ll. 19-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's FPGA to utilize Kean's CAL II FPGA and to adopt Keans's simultaneous activation of the control bits as to simultaneously turn on the interconnect elements. The artisan would be motivated to do so because it would enable Abramovici to minimize reconfiguration time reducing the cost of device testing where a large number of configurations is required.

Abramovici does not explicitly teach "said signal sources are applied to said first (second as per claim 3) end of said first (second as per claim 3) set of tracks such that adjacent tracks in said first (second as per claim 3) set of tracks have different logic values". However, Abramovici does teach output response generators 24 comparing adjacent BUT outputs. Das teaches in an analogous art "applying a set of test inputs to the adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values" in that "[t]o diagnose bridging faults between two nets (**adjacent tracks**), complementary values (**different logic values**) have to be driven on the nets and each net has to be observed at the output". (See page 267, section 2, col. 1, page 269, section "Bridging fault between two nets", col. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enhance Abramovici's FPGA interconnection testing method with Das's interconnection testing method to find stuck-at and bridging faults. The artisan would be motivated to do so because it would enable Abramovici to fully test the

programmable interconnect exactly as it will be used in system operation. Bridging faults between all pairs of nets are both detected and located greatly increasing the dependability of Abramovici's reconfigurable system (FPGA) with low cost. (See Das, page 270, section 6. Conclusions).

6. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici et al. (US-6108806), hereinafter Abramovici, in view of Wells et al. (US-6651238), hereinafter Wells, in further view of Andrews et al. (US-6064225), hereinafter Andrews, in even further view of Kean (US-6292018), hereinafter Kean, in view of Das et al. (A Low Cost Approach for Detecting, Locating, and Avoiding Interconnect Fault in FPGA-Based Reconfigurable Systems), hereinafter Das.

Claim 4:

Abramovici teaches that the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU and a second BTU, which have separate test pattern generators 20 driving each one. Abramovici illustrates in FIG. 4a, the direction of the flow of test patterns is top to bottom (vertical tracks) and the extra PLBs in row R_5 are utilized as extra output response analyzers. Abramovici also teaches test pattern generators 20 which generate test patterns (plurality of signal sources) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici further teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response. Abramovici also teaches the third and seventh

rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (producing expected output values) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col 4, lines 25-30, 44-55; Col. 5, lines 20-22; Col 6, lines 1-5, 17-23, 30, 31, 46-52). Abramovici does not explicitly teach NOR and NAND circuits for producing expected output values. However, Abramovici does teach that each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (producing expected output). Wells teaches a logic gate tree that is formed of AND and OR gates to detect stuck-at-one faults and stuck-at-zero faults (produce expected results). Wells further suggest in another embodiment of the invention, other logic gates, such as NAND and NOR gates, replace the AND and OR gates in the logic gate tree designs. (Col. 2, lines 47-55; col. 14, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's OR circuit to incorporate Wells' NAND and NOR gates. The artisan would have been motivated to do so because this would enable Abramovici to detect stuck-at-one faults and stuck-at-zero

faults rather than just stuck-at-zero faults. Abramovici teaches that a field programmable gate array (FPGA) is a type of integrated circuit consisting of an array of programmable logic blocks (PLBs) interconnected by programmable routing resources and programmable I/O cells (plurality of interface groups (IGs)) and, in programming these logic blocks, routing resources and I/O cells is selectively completed to make the necessary interconnections (provide signals to said routing circuitry) that establish a configuration thereof to provide desired system operation/function for a particular circuit application. (Col. 1, ll. 21-28). Abramovici does not explicitly teach "each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile" and "a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs". Abramovici does teach, as stated above, the FPGA consists of PLBs and programmable I/O cells (plurality of interface groups (IGs)). Andrews teaches a conventional field programmable gate array (FPGA) 100, consisting of an array of programmable logic cells (PLCs) 102 surrounded by a ring of programmable input/output (I/O) cells (PICs) 104 (plurality of interface groups (IGs)), where the PICs handle the flow of data into and out of the PLC array (provide signals to said routing circuitry). Andrews also teaches each PIC has four pads (e.g., 210) connected to the inputs of a four-to-one mux (e.g., 212) (each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers). Andrews further teaches for each PIC, the output of the mux is connected to a global-signal spine (e.g., 214) that carries global signals from the

PIC to perpendicular branches (e.g., 216) that correspond to rows in the PLC array and provide programmable connections to the individual PLCs (provide signals to said routing circuitry). (Col. 1, ll. 10-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's programmable I/O cells (IGs) with Andrews' PICs. The artisan would have been motivated to do so because this would enable Abramovici to selectively route signals from outside of the FPGA to the PLCs and other programmable logic blocks.

Abramovici does not explicitly teach providing a global control signal which turns on all interconnect elements simultaneously. However, Abramovici does teach the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU (first set of tracks) and a second BTU (second set of tracks), which have separate test pattern generators 20 driving each one. Abramovici also teaches communicating of test patterns generated by the test pattern generators to the programmable logic blocks under test by global routing (global control signals). Kean teaches in an analogous art a global control signal which turns on all interconnect elements simultaneously of a CALII FPGA which supports arrangement of the control store and the use of the wildcard registers and shift and mask registers which minimizes the number of microprocessor instructions required to access device resources and status. The specific structure of the control store allows many control bits to be written simultaneously instead of one at a time because of the structured set of data in the RAM. (Col. 43, ll. 52-66, col. 29, ll. 31-40, col. 7, ll. 39-43, col. 25, l. 63 to col. 26, l. 25, col 28, ll. 19-49). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's FPGA to utilize Kean's CAL II FPGA and to adopt Keans's simultaneous activation of the control bits as to simultaneously turn on the interconnect elements. The artisan would be motivated to do so because it would enable Abramovici to minimize reconfiguration time reducing the cost of device testing where a large number of configurations is required.

Abramovici does not explicitly teach "said signal sources are applied to said first end of said vertical tracks such that adjacent tracks in said vertical tracks have different logic values". However, Abramovici does teach output response generators 24 comparing adjacent BUT outputs. Das teaches in an analogous art "applying a set of test inputs to the adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values" in that "[t]o diagnose bridging faults between two nets (**adjacent tracks**), complementary values (**different logic values**) have to be driven on the nets and each net has to be observed at the output". (See page 267, section 2, col. 1, page 269, section "Bridging fault between two nets", col. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enhance Abramovici's FPGA interconnection testing method with Das's interconnection testing method to find stuck-at and bridging faults. The artisan would be motivated to do so because it would enable Abramovici to fully test the programmable interconnect exactly as it will be used in system operation. Bridging faults between all pairs of nets are both detected and located greatly

increasing the dependability of Abramovici's reconfigurable system (FPGA) with low cost. (See Das, page 270, section 6. Conclusions).

Claim 5:

Abramovici teaches the floor plan for the second test session shown in FIG. 4b is obtained by flipping the floor plan for the test session shown in FIG. 4a around the horizontal axis (horizontal tracks) shown as a horizontal line between rows R_4, R_5 in the middle of the array. (Col. 6, lines 52-56).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
10/11/06
John J. Tabone, Jr.
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100